REMARKS

Claims 1-24 are pending.

While the Applicants do not necessarily agree with the Examiner that identifying elements in a claim must entail a first element before a second element may be recited, the Applicants have amended Claims 5, 6, 13, 14, 21 and 22 to remove the language which the Examiner believes justifies an indefiniteness rejection. Therefore, the rejections of Claims 5, 6, 13, 14, 21, and 22 under *35 U.S.C. § 112*, second paragraph, as being indefinite are traversed.

Claim 20 has been amended to correctly depend on Claim 19.

Claims 7, 15 and 23 have been amended to correct an informality to clarify "selected sequence" from independent Claims 1, 9 and 17, respectively.

The Applicants respectfully assert that the amendments to Claims 5, 6, 7, 13, 14, 15, 21, 20, 22, and 23 and incorporated by reference in any claims depending therefrom, are not narrowing amendments made for a reason related to the statutory requirements for a patent that will give rise to prosecution history estoppel. *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 122 S. Ct. 1831, 1839-40, 62 U.S.P.Q.2d 1705, 1711-12 (2002); 234 F.3d 555, 566, 56 U.S.P.Q.2d 1865, 1870 (Fed. Cir. 2001).

I. REJECTION UNDER 35 U.S.C. § 103(a)

The Examiner rejected Claims 1-4 and 7-8 under *35 U.S.C. § 103(a)* as being unpatentable over U.S. Patent 5,418,599 to *Nakao* (hereafter *Nakao*) in view of U.S. Patent 5,434,525 to *Leonowich* (hereafter *Leonowich*) and further in view of U.S. Patent 5,815,043 to *Chow et al.* (hereafter *Chow*). The Examiner rejected Claims 9-12 and 15-16 under *35 U.S.C. § 103(a)* as being unpatentable over *Chow* in view of *Nakao* and further in view of *Leonowich*. The Examiner rejected Claims 17-20 and 23-24 under *35*

U.S.C. § 103(a) as being unpatentable over *Leonowich* in view of *Nakao* and further in view of *Chow*.

To establish a *prima facie* case of obviousness, the Examiner must meet three basic criteria. First, there must be some suggestion or motivation; either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be some reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claim limitations.

A. Rejection of Claims 1-4 and 7-8.

Claim 1 recites a ring oscillator circuit comprising a series connection of an odd number K of logic inverter gates, wherein K is greater than three, a forward conduction circuit having a first input, a first output, and receiving control inputs, said forward conduction circuit coupled in parallel with a selected sequence of logic inverter gates within said K logic inverter gates and a selectable inverter circuit, having a first inverter input, a first inverter output and receiving a first mode control signal and a second mode control signal, said first inverter input coupled to a logic input of an Nth logic inverter gate and said first inverter output coupled to a logic output of said Nth logic inverter gate, said Nth logic inverter gate selected from said K logic inverter gates, wherein a frequency range of said multi-mode VCO is selected in response to states of said first and second mode control signals.

The Examiner states that *Nakao* discloses a multi-mode VCO and cites that *Nakao* discloses a ring oscillator with an odd number (N>=3) of delay stages (logic inverter gates, G1-Gn). The Applicants do not dispute that *Nakao* discloses a multi-mode VCO, however, the Applicants assert that *Nakao* does not disclose the multi-mode VCO of Claim 1. For the invention of Claim 1 to be obvious over *Nakao*, *Nakao* must teach or suggest all the limitations of Claim 1. The Examiner states that *Nakao* discloses "forward conduction circuits (TF11, IG11) with first input and output (nodes coupling

output of G3 and G1) and control inputs being the gate terminals of TF11. The Applicants assert that TF11 and IG11 are not forward conduction circuits but rather are feedback circuits. For a circuit to be forward conduction, the output of an earlier gate (e.g., G1, G2 or G3) of *Nakao* would need to be coupled with a transfer gate to an input of a later gate (e.g., G4 and G5). As one can easily see, this is not the case. The only gates with outputs that are coupled anywhere are G3 and G5. For the circuit coupled to the output of G3 to be forward conduction, the circuit would need to couple around at least one gate whose input is coupled to the output of G3. If transfer gate TF1 is ON, the gates G4 and G5 are no longer in the oscillator loop, rather, they act as buffer circuits for the output of G3. *See* Abstract of *Nakao*. In this case, the input of G3 receives a signal from the output of G2 and the output of G3 feeds back to the input of G1. G1, G2 and G3 form an odd number of gates. G1, G2 and G3, singly, also form an odd number of gates (in this case 1). A circuit coupling the output of G1 to the input of G3, the output of G2 to the input of G1 and the output of G3 to the input of G2 would be forward conduction circuits. Clearly this is not taught or suggested in *Nakao*. Likewise, a forward conduction circuit would couple the output of a first gate (e.g., G1) around the next odd number (3) sequentially coupled gates (G2-G4) to the input of G5. Other examples of forward conduction circuits using *Nakao* would couple the output of G2 to the input of G1, the output of G3 to the input of G2, the output of G4 to the input of G3 and finally the output of G5 to the input of G4. It should be clear that none of these forward conduction couplings are taught or suggested by *Nakao*. *Nakao* only shows a transfer gate TF1 coupling the output of G3 to the input of G1 when TF1 is ON and TF2 is OFF. In this case, TF1 does not bypass an odd number of series connected gates coupled to the output of G3. G4, G5, and G1 are the three series connected gates coupled to the output of G3 and when TF1 is ON, they act as buffers and are not in the oscillator loop. Transfer gate TF1 makes the connection between the output of G5 and the input of G1. There is no odd number of gates coupled in series with the output of G5, therefore, transfer gate TF2 cannot function to forward conduct around any odd number of gates connected to the only other possible path suggested and taught by *Nakao*. Rather

Nakao is teaching two possible feedback paths which serve to couple either three or five gates in series.

The Examiner admits that *Nakao* does not teach the selectable inverter circuit, having a first inverter input, a first inverter output and receiving a first mode control signal and a second mode control signal, said first inverter input coupled to a logic input of an Nth logic inverter gate and said first inverter output coupled to a logic output of said Nth logic inverter gate, said Nth logic inverter gate selected from said K logic inverter gates. The Examiner further states that *Leonowich* is silent regarding a selectable inverter circuit. However, the Examiner states that *Chow* is "relied upon for suggesting that the parallel connected inverter circuits may indeed be selectable, i.e., via the transfer gates (see *Chow* FIGS. 7 and 8)." FIG. 7 of *Chow* only shows series connected delay stages wherein each delay stage has a different amount of delay. See *Chow*, column 8, lines 16-44. Nowhere in FIG. 7 does *Chow* teach or suggest an odd number K of series connected inverter stages forming a ring oscillator. Selectable inverter circuits do not bypass the delay stages shown in FIG. 7 of *Chow*, rather, *Chow* teaches bypassing the non-inverting delay stages with a bypass switch. Since the delay stages of *Chow* are non-inverting, *Chow* cannot teach or suggest a selectable inverter paralleling inverting stages in a ring oscillator. Nowhere does *Chow* teach or suggest the use of a selectable inverter circuit as recited in Claim 1 of the present invention. FIG. 8 of *Chow* shows that the bypass switch used in FIG. 7 may be a non-inverting transfer gate. FIG. 8 adds nothing to the disclosure of FIG. 7 relied on by the Examiner to support his assertion that *Chow* teaches the selectable inverter circuit of Claim 1. Rather, FIG. 8 simply illustrates how to implement a non-inverting bypass switch.

In several instances, the Examiner makes statements about items being inherent. The Examiner states that Leonowich discloses a PLL with differential phase detector and inherent charge pump output signals (albeit not shown) coupled to the ring oscillator to allow for the frequency control as desired (via VCN, VCP mode control signals), note inherently, there will be intrinsic capacitance and ultimately delay stage capacitance on

each pump out line. *Leonowich* does not show a charge pump and there is not reason to assume that a charge pump is inherent to the teachings of *Leonowich*. The Examiners note that "inherently, there will be intrinsic capacitance and ultimately delay stage capacitance on each pump out line", is irrelevant to the argument whether the combination of *Nakao* and *Leonowich* teach or suggest the invention of Claim 1 which makes no mention of capacitance.

The Examiner has admitted that *Nakao* and *Leonowich* do not teach or suggest all of the limitations of the invention of Claim 1. The Examiner relies on *Chow* to teach the selectable inverter circuit of Claim 1. The Applicants have shown that *Chow* does not teach or suggest the use of a selectable inverter circuit as recited in Claim 1 of the present invention. The Examiner has shown no motivation for combining the teachings of *Nakao*, *Leonowich,* and *Chow* to arrive at the invention of Claim 1. The Applicants, therefore, respectfully assert that the rejection of Claim 1 as being obvious under *35 U.S.C. § 103(a)* as being unpatentable over *Nakao* in view of *Leonowich* and further in view of *Chow* is traversed at least for the reasons stated above.

Claim 2 is dependent from Claim 1 and further limits the selectable inverter of Claim 1. The Applicants have shown that *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest the invention of Claim 1. Specifically, *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest a selectable inverter coupled in parallel with a series connected inverter stage of the ring oscillator of Claim 1. Thus the references, singly or in combination necessarily fail to teach or suggest the selectable inverter of Claim 2. Neither is there a motivation to modify one reference to make the invention of Claim 2. The Applicants, therefore, respectfully assert that the rejection of Claim 2 as being obvious under *35 U.S.C. § 103(a)* as being unpatentable over *Nakao* in view of *Leonowich* and further in view of *Chow* is traversed.

Claim 3 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 3 further limits the forward conduction circuit of Claim 1. The Applicants have shown that *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or

suggest the invention of Claim 1. Specifically, *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest a selectable inverter coupled in parallel with a series connected inverter stage of the ring oscillator of Claim 1. Thus the references, singly or in combination necessarily fail to teach or suggest the selectable inverter of Claim 3. Neither is there a motivation to modify one reference to make the invention of Claim 3. The Applicants, therefore, respectfully assert that the rejection of Claim 3 as being obvious under *35 U.S.C. § 103(a)* as being unpatentable over *Nakao* in view of *Leonowich* and further in view of *Chow* is traversed at least for the same reasons as Claim 1 and for the reasons stated above.

Claim 4 is dependent from Claim 3 and contains all the limitations of Claim 3 and Claim 1. Claim 4 further limits the bi-direction conduction circuit of Claim 3. The Applicants have shown that *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest the invention of Claim 1. Specifically, *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest a selectable inverter coupled in parallel with a series connected inverter stage of the ring oscillator of Claim 1. Thus the references, singly or in combination necessarily fail to teach or suggest the selectable inverter of Claim 4. Neither is there a motivation to modify one reference to make the invention of Claim 4. The Applicants, therefore, respectfully assert that the rejection of Claim 4 as being obvious under *35 U.S.C. § 103(a)* as being unpatentable over *Nakao* in view of *Leonowich* and further in view of *Chow* is traversed at least for the same reasons as Claim 3 and for the reasons stated above.

Claim 7 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 1 recites that the forward conduction circuit is coupled in parallel with a selected sequence of inverter gates from the series connected K logic gates making up the ring oscillator. Claim 7 further limits the selected sequence from the K logic inverter gates to comprise three inverter logic gates. The Applicants have shown that *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest the invention of Claim 1. Specifically, *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not

teach or suggest a selectable inverter coupled in parallel with a series connected inverter stage of the ring oscillator of Claim 1. Thus the references, singly or in combination necessarily fail to teach or suggest the selectable inverter of Claim 7. Neither is there a motivation to modify one reference to make the invention of Claim 7. The Applicants, therefore, respectfully assert that the rejection of Claim 7 as being obvious under *35 U.S.C. § 103(a)* as being unpatentable over *Nakao* in view of *Leonowich* and further in view of *Chow* is traversed at least for the same reasons as Claim 1 and for the reasons stated above.

Claim 8 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 8 further limits each of said K inverter logic gates of said ring oscillator to be coupled in parallel with a corresponding one of said selectable inverter circuits. The Applicants have shown that *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest the invention of Claim 1. Specifically, *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest a selectable inverter coupled in parallel with a series connected inverter stage of the ring oscillator of Claim 1. Thus the references, singly or in combination necessarily fail to teach or suggest the selectable inverter of Claim 8. Neither is there a motivation to modify one reference to make the invention of Claim 8. The Applicants, therefore, respectfully assert that the rejection of Claim 8 as being obvious under *35 U.S.C. § 103(a)* as being unpatentable over *Nakao* in view of *Leonowich* and further in view of *Chow* is traversed at least for the same reasons as Claim 1 and for the reasons stated above.

B. Rejection of Claims 9-12 and 15-16.

The Examiner rejected Claims 9-12 and 15-16 under *35 U.S.C. § 103(a)* as being unpatentable over *Chow* in view of *Nakao* and further in view of *Leonowich*.

Claim 9 recites a data processing system comprising a central processor unit (CPU), operable to generate a clock signal with a phase lock loop (PLL) clock generator having a ring oscillator circuit configured as a series connection of an odd number K of

logic inverter gates, wherein K is greater than three, a forward conduction circuit having a first input, a first output, and receiving control inputs, said forward conduction circuit coupled in parallel with a selected sequence from said K logic inverter gates, and a selectable inverter circuit, having a first inverter input, a first inverter output and receiving a first mode control signal and a second mode control signal, said first inverter input coupled to a logic input of an Nth logic inverter gate and said first inverter output coupled to a logic output of said Nth logic inverter gate, said Nth logic inverter gate selected from said K logic inverter gates, a random access memory (RAM), a read only memory (ROM), an I/O adapter, and a bus system coupling said CPU to said ROM, said I/O adapter, and said RAM, wherein a frequency range of said ring oscillator circuit is selected in response to states of said first and second mode control signals. All the limitations of Claim 9 must be taught or suggested for a single or combination of references to render a claim obvious. The Applicants have shown in FIGS. 1 and 2 of the present disclosure prior art ring oscillator circuits that comprises an odd number K of series connected inverters and forward conduction circuit coupled in parallel with a selected sequence from said K logic inverter gates. What the prior art does not teach or suggest is the addition of a selectable inverter circuit, having a first inverter input, a first inverter output and receiving a first mode control signal and a second mode control signal, said first inverter input coupled to a logic input of an Nth logic inverter gate and said first inverter output coupled to a logic output of said Nth logic inverter gate, said Nth logic inverter gate selected from said K logic inverter gates. Claim 9 recites a specific data processing system having a PLL with a ring oscillator with the same limitation as recited in Claim 1. The Applicants have shown that *Chow*, *Nakao*, and *Leonowich*, singly and in combination do not teach or suggest the invention of Claim 1. Clearly the same references cannot teach or suggest a data processing system having a PLL with a ring oscillator with the same limitations recited in Claim 1.

The Examiner states that *Chow* teaches the computer system of Claim 9 and cites FIGS. 2 and 4 of *Chow*. FIG 2 of *Chow* illustrates only a CPU 202 and its connections to a DRAM memory 204, a corresponding memory controller 208, a crystal oscillator

214 and a power manager 218. *Chow* is describing how the computer system of FIG. 2 can be put into a sleep mode where the crystal oscillator 214 is shut down. In this mode, *Chow* states that an internal clock (not shown) to the memory controller 208 is a ring oscillator according to the invention of *Chow*. The only ring oscillator disclosed by *Chow* is described relative to FIG. 7. FIG. 7 discloses a ring oscillator comprising six non-inverting delay elements with varying delay (702, 704, 706, 708, 710, and 712), one inverting logic gate 714, and an OR logic gate 730. The Examiner states that *Chow* shows "in FIGS. 4, 7, and 8, selecting a particular transfer gate to increase/decrease the frequency is achieved and each gate is coupled in parallel with a respective inverter stage." FIG. 7 shows only one inverter stage, inverter 714. The other stages in FIG. 7 are non-inverting delay elements with varying delay, 702, 704, 706, 708, 710, and 712. These non-inverting delay elements are shown in parallel with a bypass switch, which "eliminates" the delay of its delay element when it is ON. See *Chow*, column 8, lines 29-33. Clearly *Chow* does not teach or suggest the data processing system of Claim 9 where the CPU generates a clock signal using a PLL having the ring oscillator of Claim 9. *Chow* does not teach or suggest the ring oscillator in the computer system of Claim 9. *Chow* specifically states that "the ring oscillator 402 is constructed with the delay stages according to FIG. 7 and the bypass switches according to FIG. 8. *See Chow*, column 7, lines 65-67. *Chow* further states that "the ring oscillator according to the invention is able to be used in a computer system for the purpose timing the refreshing of DRAM." *See Chow* column 9, lines 22-24. *Chow* then states that "the ring oscillator also has significantly lower cost and lower power consumption than does a phase-locked loop (PLL) or crystal based oscillator". See *Chow*, column 9, lines 24-27. The ring oscillator of *Chow* is used only for refreshing the DRAM and is not part of a PLL as recited in the invention of Claim 9.

The Applicants do not dispute that *Nakao* discloses a ring oscillator. The Applicants have shown that *Nakao* does not teach or suggest a ring oscillator with the limitation of a selectable inverter circuit, having a first inverter input, a first inverter output and receiving a first mode control signal and a second mode control signal, said

first inverter input coupled to a logic input of an Nth logic inverter gate and said first inverter output coupled to a logic output of said Nth logic inverter gate, said Nth logic inverter gate selected from said K logic inverter gates as recited in Claim 1 and Claim 9 of the present invention.

The Examiner states that *Leonowich* discloses a PLL with a differential phase detector using inverter gates connected in parallel (using voltage variable transfer gates) across the ring oscillator delay stages. The Applicants do not dispute this assertion as FIG. 2 in the disclosure of the present invention also shows the prior art circuit in FIG. 1 of *Leonowich*. What *Leonowich* does not teach or suggest is a ring oscillator with the limitation of a selectable inverter circuit, having a first inverter input, a first inverter output and receiving a first mode control signal and a second mode control signal, said first inverter input coupled to a logic input of an Nth logic inverter gate and said first inverter output coupled to a logic output of said Nth logic inverter gate, said Nth logic inverter gate selected from said K logic inverter gates as recited in Claim 1 and Claim 9 of the present invention. The Applicants, therefore, respectfully assert that the rejection of Claim 9 as being obvious under *35 U.S.C. § 103(a)* as being unpatentable over *Chow* in view of *Nakao* and further in view of *Leonowich* is traversed at least for the same reasons as Claim 1 and for the reasons stated above.

Claim 10 is dependent from Claim 9 and contains all the limitations of Claim 9. Claim 10 further limits the selectable inverter of Claim 9. The Applicants have shown that *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest the invention of Claim 9. Specifically, *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest a selectable inverter coupled in parallel with a series connected inverter stage of the ring oscillator of Claim 9. The Applicants, therefore, respectfully assert that the rejection of Claim 10 as being obvious under *35 U.S.C. § 103(a)* as being unpatentable over *Nakao* in view of *Leonowich* and further in view of *Chow* is traversed at least for the same reasons as Claim 1, Claim 9, and for the reasons stated above.

Claim 11 is dependent from Claim 9 and contains all the limitations of Claim 9. Claim 11 further limits the forward conduction circuit of Claim 9. The Applicants have shown that *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest the invention of Claim 9. Specifically, *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest a selectable inverter coupled in parallel with a series connected inverter stage of the ring oscillator of Claim 9. The Applicants, therefore, respectfully assert that the rejection of Claim 11 as being obvious under *35 U.S.C. § 103(a)* as being unpatentable over *Nakao* in view of *Leonowich* and further in view of *Chow* is traversed at least for the same reasons as Claim 1, Claim 9, and for the reasons stated above.

Claim 12 is dependent from Claim 11 and contains all the limitations of Claim 11 and Claim 9. Claim 12 further limits the bi-direction conduction circuit of Claim 11. The Applicants have shown that *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest the invention of Claim 9. Specifically, *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest a selectable inverter coupled in parallel with a series connected inverter stage of the ring oscillator of Claim 9. The Applicants, therefore, respectfully assert that the rejection of Claim 12 as being obvious under *35 U.S.C. § 103(a)* as being unpatentable over *Nakao* in view of *Leonowich* and further in view of *Chow* is traversed at least for the same reasons as Claim 11, Claim 9, Claim 1, and for the reasons stated above.

Claim 15 is dependent from Claim 9 and contains all the limitations of Claim 9. Claim 9 recites that the forward conduction circuit is coupled in parallel with a selected sequence of inverter gates from the series connected K logic gates making up the ring oscillator. Claim 15 further limits the selected sequence from the K logic inverter gates to comprise three inverter logic gates. The Applicants have shown that *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest the invention of Claim 9. Specifically, *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest a selectable inverter coupled in parallel with a series connected inverter

stage of the ring oscillator of Claim 9. The Applicants, therefore, respectfully assert that the rejection of Claim 15 as being obvious under *35 U.S.C. § 103(a)* as being unpatentable over *Nakao* in view of *Leonowich* and further in view of *Chow* is traversed at least for the same reasons as Claim 9 and for the reasons stated above.

Claim 16 is dependent from Claim 9 and contains all the limitations of Claim 9. Claim 16 further limits each of said K inverter logic gates of said ring oscillator to be coupled in parallel with a corresponding one of said selectable inverter circuits. The Applicants have shown that *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest the invention of Claim 9. Specifically, *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest a selectable inverter coupled in parallel with a series connected inverter stage of the ring oscillator of Claim 9. The Applicants, therefore, respectfully assert that the rejection of Claim 16 as being obvious under *35 U.S.C. § 103(a)* as being unpatentable over *Nakao* in view of *Leonowich* and further in view of *Chow* is traversed at least for the same reasons as Claim 9 and for the reasons stated above.

C. Rejection of Claims 17-20 and 23-24.

The Examiner rejected Claims 17-20 and 23-24 under *35 U.S.C. § 103(a)* as being unpatentable over *Leonowich* in view of *Nakao* and further in view of *Chow*.

Claim 17 recites a phase lock loop (PLL) circuit comprising a phase/frequency comparator, a charge pump circuit, a voltage-controlled oscillator (VCO), and a signal frequency divider. The VCO in Claim 17 has a ring oscillator as recited in Claim 1 of the present invention. For Claim 17 to be obvious over the cited references all the limitations of Claim 17 must be taught or suggested, in particular, the VCO with the ring oscillator with the limitations of Claim 1.

While *Leonowich* discloses a PLL coupled to a ring oscillator, it is not the ring oscillator recited in Claim 17. The ring oscillator in Claim 17 has the same limitations as the ring oscillator in Claim 1. The Examiner has stated relative to Claim 1 that

Leonowich is silent on a ring oscillator with a selectable inverter circuit. Relative to Claim 17, the Examiner states that *Leonowich* does not suggest a ring oscillator circuit with a conventional forward conduction circuit nor a selectable inverter circuit. The Examiner also states that *Leonowich* does not disclose a divider in the feedback loop of the PLL. The Applicants note that *Leonowich* does show a type of feedforward circuit. What *Leonowich* does not teach or suggest is the selectable inverter circuit of Claim 1 and Claim 17.

The Examiner states that *Chow* teaches the use of a selectable inverter circuit as recited in the PLL of Claim 17 of the present invention.

The Examiner states that *Chow* discloses a computer system (FIG. 2 of *Chow*) with controlled ring oscillator within a PLL. FIG. 2 of *Chow* illustrates only a CPU 202 and its connections to a DRAM memory 204, a corresponding memory controller 208, a crystal oscillator 214 and a power manager 218. *Chow* describes how the computer system of FIG. 2 can be put into a sleep mode where the crystal oscillator 214 is shut down. In this mode, *Chow* states that an internal clock (not shown) to the memory controller 208 is a ring oscillator according to the invention of *Chow*. The only ring oscillator disclosed by *Chow* is described relative to FIG. 7. FIG. 7 discloses a ring oscillator comprising six non-inverting delay elements with varying delay (702, 704, 706, 708, 710, and 712), one inverting logic gate 714, and an OR logic gate 730. The Examiner states that *Chow* shows, "in FIGS. 4, 7, and 8, selecting a particular transfer gate to increase/decrease the frequency is achieved and each gate is coupled in parallel with a respective inverter stage. FIG. 7 shows only one inverter stage, inverter 714. The other stages in FIG. 7 are non-inverting delay elements with varying delay; 702, 704, 706, 708, 710, and 712. These non-inverting delay elements are shown in parallel with a bypass switch, which "eliminates" the delay of its delay element when it is ON. *See Chow*, column 8, lines 29-33. Clearly *Chow* does not teach or suggest using a PLL having the ring oscillator of Claim 17. *Chow* specifically states that "the ring oscillator 402 is constructed with the delay stages according to FIG. 7 and the bypass switches

according to FIG. 8." *See Chow*, column 7, lines 65-67. *Chow* further states that "the ring oscillator according to the invention is able to be used in a computer system for the purpose timing the refreshing of DRAM." See *Chow* column 9, lines 22-24. *Chow* then states that "the ring oscillator also has significantly lower cost and lower power consumption than does a phase-locked loop (PLL) or crystal based oscillator." *See Chow*, column 9, lines 24-27. The ring oscillator of *Chow* is used only for refreshing the DRAM and is not within a PLL as recited in the invention of Claim 17. *Chow* is teaching that his ring oscillator be used as a low cost and low power replacement for a PLL clock circuit. The Applicants assert that no one of ordinary skill in the art would look to *Leonowich* for a PLL circuit with a ring oscillator according to embodiments of the present invention as *Leonowich* is teaching an oscillator to be used in place of a PLL based oscillator. The Applicants, therefore, respectfully assert that the rejection of Claim 17 under *35 U.S.C. § 103(a)* as being unpatentable over *Leonowich* in view of *Nakao* and further in view of *Chow* is traversed for at least the same reasons as Claim 1, Claim 9, and for the reasons stated above.

Regarding the rejections of Claims 17-20 and 23-24, the Examiner makes statements about items being inherent. The Examiner states that Leonowich discloses a PLL with differential phase detector and inherent charge pump output signals (albeit not shown) coupled to the ring oscillator to allow for the frequency control as desired (via VCN, VCP mode control signals), note inherently, there will be intrinsic capacitance and ultimately delay stage capacitance on each pump out line. *Leonowich* does not show a charge pump and there is not reason to assume that a charge pump is inherent to the teachings of *Leonowich*. The Examiner's note that "inherently, there will be intrinsic capacitance and ultimately delay stage capacitance on each pump out line", is irrelevant to the argument whether the combination of *Nakao* and *Leonowich* teach or suggest the invention of Claim 1 which makes no mention of capacitance. The Examiner states that the reference by *Chow* discloses a computer system with controlled ring oscillator within a PLL, that includes CPU (202), DRAM (204), data bus (I/O), etc. this inherently includes access to EPROMS/ROM....." Just because a reference discloses a computer

system with certain features, there is no reason to assume that some other feature is inherent unless there is some suggestion to that affect. In either case, whether the computer system of *Chow* includes is irrelevant to the argument whether the combination of *Nakao*, *Leonowich*, and *Chow* teach or suggest the invention of Claim 17 which makes no mention access to EPROMS/ROM.

Claim 18 is dependent from Claim 17 and contains all the limitations of Claim 17. Claim 18 further limits the selectable inverter of Claim 17. The Applicants have shown that *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest the invention of Claim 17. Specifically, *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest a selectable inverter coupled in parallel with a series connected inverter stage of the ring oscillator of Claim 17. The Applicants, therefore, respectfully assert that the rejection of Claim 17 as being obvious under *35 U.S.C. § 103(a)* as being unpatentable over *Nakao* in view of *Leonowich* and further in view of *Chow* is traversed at least for the same reasons as Claim 1, Claim 9, Claim 17 and for the reasons stated above.

Claim 19 is dependent from Claim 17 and contains all the limitations of Claim 17. Claim 19 further limits the forward conduction circuit of Claim 17. The Applicants have shown that *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest the invention of Claim 17. Specifically, *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest a selectable inverter coupled in parallel with a series connected inverter stage of the ring oscillator of Claim 17. The Applicants, therefore, respectfully assert that the rejection of Claim 19 as being obvious under *35 U.S.C. § 103(a)* as being unpatentable over *Nakao* in view of *Leonowich* and further in view of *Chow* is traversed at least for the same reasons as Claim 1, Claim 9, Claim 17, and for the reasons stated above.

Claim 20 is dependent from Claim 19 and contains all the limitations of Claims 19 and Claim 17. Claim 20 further limits the bi-direction conduction circuit of Claim 11. The Applicants have shown that *Nakao*, *Leonowich*, and *Chow*, singly or in

combination, do not teach or suggest the invention of Claim 17. Specifically, *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest a selectable inverter coupled in parallel with a series connected inverter stage of the ring oscillator of Claim 17. The Applicants, therefore, respectfully assert that the rejection of Claim 20 as being obvious under *35 U.S.C. § 103(a)* as being unpatentable over *Nakao* in view of *Leonowich* and further in view of *Chow* is traversed at least for the same reasons as Claim 1, Claim 9, Claim 17, and Claim 19 and for the reasons stated above.

Claim 23 is dependent from Claim 17 and contains all the limitations of Claim 17. Claim 17 recites that the forward conduction circuit is coupled in parallel with a selected sequence of inverter gates from the series connected K logic gates making up the ring oscillator. Claim 23 further limits the selected sequence from the K logic inverter gates to comprise three inverter logic gates. The Applicants have shown that *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest the invention of Claim 17. Specifically, *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest a selectable inverter coupled in parallel with a series connected inverter stage of the ring oscillator of Claim 17. The Applicants, therefore, respectfully assert that the rejection of Claim 23 as being obvious under *35 U.S.C. § 103(a)* as being unpatentable over *Nakao* in view of *Leonowich* and further in view of *Chow* is traversed at least for the same reasons as Claim 1, Claim 17, and for the reasons stated above.

Claim 24 is dependent from Claim 17 and contains all the limitations of Claim 17. Claim 24 further limits each of said K inverter logic gates of said ring oscillator to be coupled in parallel with a corresponding one of said selectable inverter circuits. The Applicants have shown that *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest the invention of Claim 17. Specifically, *Nakao*, *Leonowich*, and *Chow*, singly or in combination, do not teach or suggest a selectable inverter coupled in parallel with a series connected inverter stage of the ring oscillator of Claim 17. The Applicants, therefore, respectfully assert that the rejection of Claim 24 as being obvious

under *35 U.S.C. § 103(a)* as being unpatentable over *Nakao* in view of *Leonowich* and further in view of *Chow* is traversed at least for the same reasons as Claim 1, Claim 17, and for the reasons stated above.

The Examiner states that "in light of his arguments it would have been obvious to one of ordinary skill in the art to have modified the PLL circuit of *Leonowich* to include conventional frequency control means such as the output divider for dividing the VCO output as desired as well as the forward conduction circuit by *Nakao* to allow for enhanced frequency control. The implementation of selectable transfer gate/inverter circuit is shown by chow also enhancing the frequency of the VCO." There is no motivation in any of the cited references to make such combinations. This is a broad, conclusory statement regarding teaching of references. Teachings must be clear and particular, and broad conclusory statements regarding the teachings standing alone are not evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1616 (Fed. Cir. 1999). The factual question of motivation is material to patentability and cannot be resolved on subjective belief and unknown authority. *In re Lee*, 277 F.3d at 1343-44, 61 U.S.P.Q.2d at 1434.

III. CONCLUSION

Amending Claim 20 as suggested by the Examiner overcomes the objection to Claim 20. Claims 5, 6, 13, 14, 21, and 22 have been amended to overcome the rejections under *35 U.S.C. § 112*, second paragraph, as being indefinite.

The rejections of Claims 1-4 and 7-8 under *35 U.S.C. § 103(a)* as being unpatentable over *Nakao* in view of *Leonowich* and further in view of *Chow* are overcome. The rejections of Claims 9-12 and 15-16 under *35 U.S.C. § 103(a)* as being unpatentable over *Chow* in view of *Nakao* and further in view of *Leonowich* are overcome. The rejections of Claims 17-20 and 23-24 under *35 U.S.C. § 103(a)* as being unpatentable over *Leonowich* in view of *Nakao* and further in view of *Chow* are overcome.

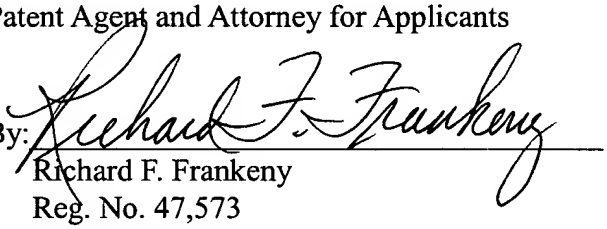
The Applicants, therefore, respectfully assert that Claims 1-24 are now in condition for allowance and request an early allowance of these claims.

Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

WINSTEAD SECHREST & MINICK P.C.

Patent Agent and Attorney for Applicants

By: 

Richard F. Frankeny
Reg. No. 47,573
Kelly K. Kordzik
Reg. No. 36,571

P.O. Box 50784
1201 Main Street
Dallas, Texas 75250-0784
(512) 370-2872